<u>In the Claims</u>

Replace claims 1, 16, 23, and 30 as follows:

1   1. (once amended)   A method of providing ordered data transmitted from a data source

2   to a data destination over a bus, comprising the steps of:

3   writing items of data into sequentially ordered areas of a memory, the items of

4   data having a predefined order in the data source, the sequentially ordered areas of

5   memory being identifiable by addresses, each item of data being placed in an area having

6   an associated address in the data source;

7   transmitting the items of data and associated addresses from the data source to the

8   data destination over the bus, the items of data being transmitted in an order other than

9   the predefined order;

10   receiving the items of data and the associated addresses in the data source from

11   the bus;

12   examining the associated address in the data source for each item of data received

13   from the bus; and

14   placing each item of data received from the bus in one of multiple sequentially

15   arranged areas of a storing buffer, each item being placed based on the associated address

16   in the data source for each item, the placement of the items of data causing reordering of

17   the received items of data.

1 16. (once amended) A bus interface unit of a computer device, the bus interface unit

2 being coupled to a bus with a weakly ordered interface providing information comprised

3 of data items and associated addresses received from a data source, the bus interface unit

4 comprising:

5   a plurality of storage buffers each having a plurality of slots for storing data items,

6 the plurality of slots being identifiable by addresses;

7   a first router for routing the data items received from the bus to a particular one of

8 the plurality of storage buffers based on a first part of the addresses in the data source

9 associated with the data items; and

10   a plurality of second routers for each of the storage buffers for routing the data

11 items routed to the particular one of the storage buffers to one of the slots in the particular

12 one of the storage buffers based on a second part of the addresses in the data source

13 associated with the data items.

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1 23. (once amended) A computer device for reordering incoming data received from a

2 data source over a bus interface, the incoming data having a predefined order and

3 associated address information in the data source, comprising:

4   a receive buffer which receives the incoming data and the associated address

5 information in the data source, the received incoming data being out of the predefined

6 order;

7   a storage buffer which stores the incoming data in an order based on the

8 associated address information in the data source; and

9   a detector which determines proper placement of the out order incoming data in

10 the receive buffer in the storage buffer based on the associated address information in the

11 data source to reorder the out order incoming data.

1   30. (once amended) A method of reordering incoming data transmitted from a data

2   source to a data destination, the incoming data containing address information in the data

3   source, the incoming data being in a predefined order in the data source and being

4   transmitted from the data source to the data destination in an order other than the

5   predefined order, the method comprising the steps of:

6   receiving at the data destination the incoming data and the address information

7   transmitted from the data source;

8   arranging, in the predefined order, the incoming data based on the address

9   information in the data source contained within the incoming data; and

10   storing the arranged data temporarily.

Please reinstate claims 14-15, which were previously removed from examination, as follows:

1 14. (reinstated and once amended) A method of increasing effective bus bandwidth for
2 transmitting items of data from a data source to a data destination, comprising the steps
3 of:
4   defining a region of a memory as a write combining memory type, the region of
5 the memory being comprised of addressable locations of processor memory, the
6 addressable locations identifiable by addresses in the data source;
7   writing items of data into the region in a sequential order of the addressable
8 locations, the items of data comprising encoded commands and parameters associated
9 with the encoded commands, the items of data having a predefined order in the data
10 source;
11   transmitting the items of data and addresses of the items of data from the data
12 source to the data destination over a bus, the items of data being transmitted in an order
13 other than the predefined order; and
14   arranging the transmitted items of data in an order corresponding to the addresses
15 in the data source for the items of data to reorder the transmitted items of data.

1   15. (reinstated and once amended) The method of increasing effective bus bandwidth of

2   claim 14 further comprising the steps of determining which items of data in the order

3   corresponding to the sequential order of addressable locations are encoded commands and

4   further determining which parameters are associated with each encoded command and the

5   meaning of the parameters based on their position in the order of addressable locations.